Computer Architecture & Embedded Systems Education and Research

Prof. Dr.
Sezer GÖREN UĞURDAĞ
Department Chair
Computer Engineering
Yeditepe University

Part1: Background

Education

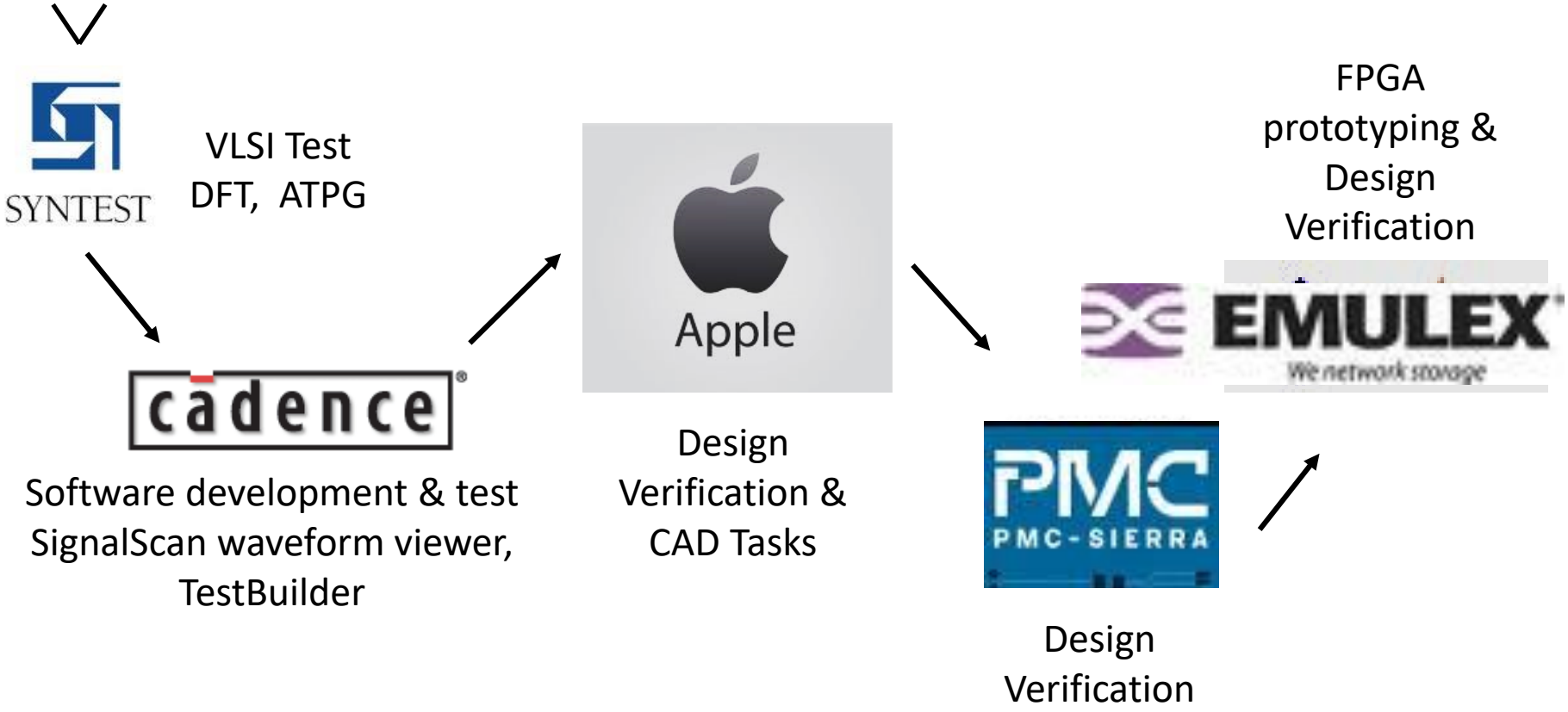
BS & MS in EEE (1988-1995)
VLSI Implementation of Morphological Filters
Advisor: Prof. Sina Balkır

Research Fellow (1996)
FPGA Implementation of Advanced Morphological Filters
Prof. Jean Serra, J. C. Klein

UNIVERSITY OF CALIFORNIA
SANTA CRUZ

PhD in CSE (1997-2003)
VLSI Test
Supervisor:
Prof. F. Joel FERGUSON

Silicon Valley 1997-2005



Part2: Teaching

2005-ongoing

- Introduction to Digital Electronics
- Analysis of Algorithms
- Embedded Systems Programming
- Intro. To Automotive Software Engineering
- Reconfigurable Computing
- Digital System Design
- Microprocessors & Microcontrollers
- Principles of Logic Design
- Real Time Systems

RESysLab @ Yeditepe University
Reconfigurable & Embedded Systems Lab.

Uploads

Robot Arm Platform with MSP430
30 views • 3 months ago

ADXL345 and ITG-3200 Integrated with BeagleBone Black
52 views • 10 months ago

A Wearable Device for Personal Activity Tracking (designed by.
32 views • 10 months ago

Rechargable Battery Based on Self Moving Solar Panel.
34 views • 10 months ago

Remote-Controlled Smart Power Sockets (designed by Efe Andac)
41 views • 10 months ago

Mobile Map Builder (designed by Firdevs Gizem Basaran)
64 views • 1 year ago

Embedded Home Security and Automation System (designed b..
44 views • 2 years ago

Piewer (designed by Gozde Karakas)
72 views • 2 years ago

SoftPot-Driven DC Motor Controller
57 views • 2 years ago

UART Controlled Framebuffer
80 views • 2 years ago

Part3: Research

Interests

- Hardware Security
- High Performance Arithmetic Circuits
- Digital Design
- Reconfigurable Computing
- Vehicular Technologies
- Embedded Systems
- VLSI Test
- EDA for Nanoelectronics
- Machine Vision
- IoT
- Smart City

VSCPU- working CPU on FPGA

- Assembler
- Instruction Set Simulator (ISS)
- Web-based ISS
- C compiler
- PIC16 to VSCPU assembly converter
- FPGA debug interface
- Worst Case Execution Time (WCET) profiler
- Hundreds of synthesizable Verilog implementations (including pipelined versions)
- Several peripherals
- Several customized versions

VSCPU v1 Instruction Set

Instruction	Description	Functionality
`ADD A B`	`ADDition`	`*A = *A + *B`
`NAND A B`	`bitwise NAND`	`*A = ~(*A & *B)`
`SRL A B`	`Shift Right or Left`	`*A = (*B < 32) ? (*A >> *B) : (*A << (*B-32))`
`LT A B`	`Less Than`	`*A = *A < *B`
`CP A B`	`CoPy`	`*A = *B`
`CPI A B`	`CoPy Indirect`	`*A = **B`
`CPIi A B`	`CoPy Indirect immediate`	`**A = *B`
`BZJ A B`	`Branch on Zero or Jump`	`PC = (*B == 0) ? *A : (PC + 1)`

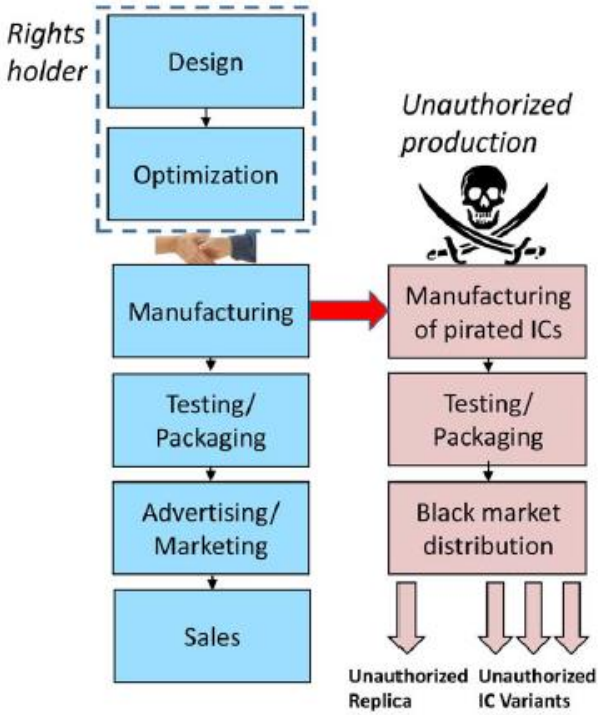
Multi-Core Microcontroller Synthesis

- CPU Design Simplified
- Software UART: A Use Case for VSCPU Worst-Case Execution Time Analyzer
- Fast and Efficient Implementation of Lightweight Crypto Algorithm PRESENT on FPGA through Processor Instruction Set Extension

Third Shift Problem in IC Industry

Outsourcing fabrication

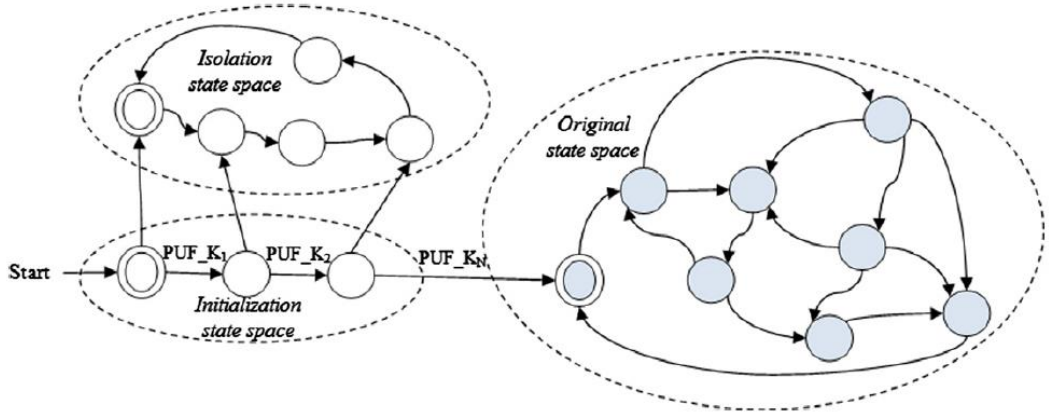
- foundries can overproduce chips, distribute them on the black market
- create unauthorized IC variant designs by slightly modifying original masks.

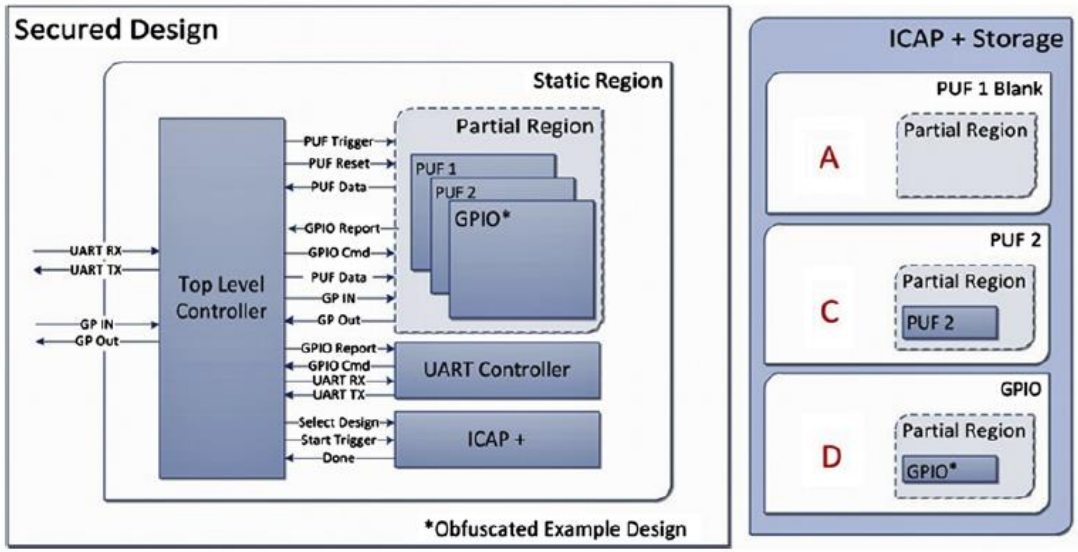


Hardware Security

- Protect ICs from
  - Theft
  - Cloning
  - Reverse engineering
  - Overbuilding
  - Trojans
  - Piracy
- Techniques to Protect ICs
  - Obfuscation
  - Logic Locking
    - Combinational
    - Sequential
  - Physically Unclonable Functions (PUFs)

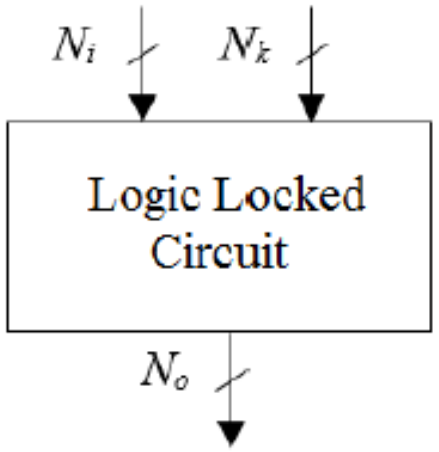
Partial Bitstream Protection for Low-Cost FPGAs with Physical Unclonable Function, Obfuscation, and Dynamic Partial Self Reconfiguration



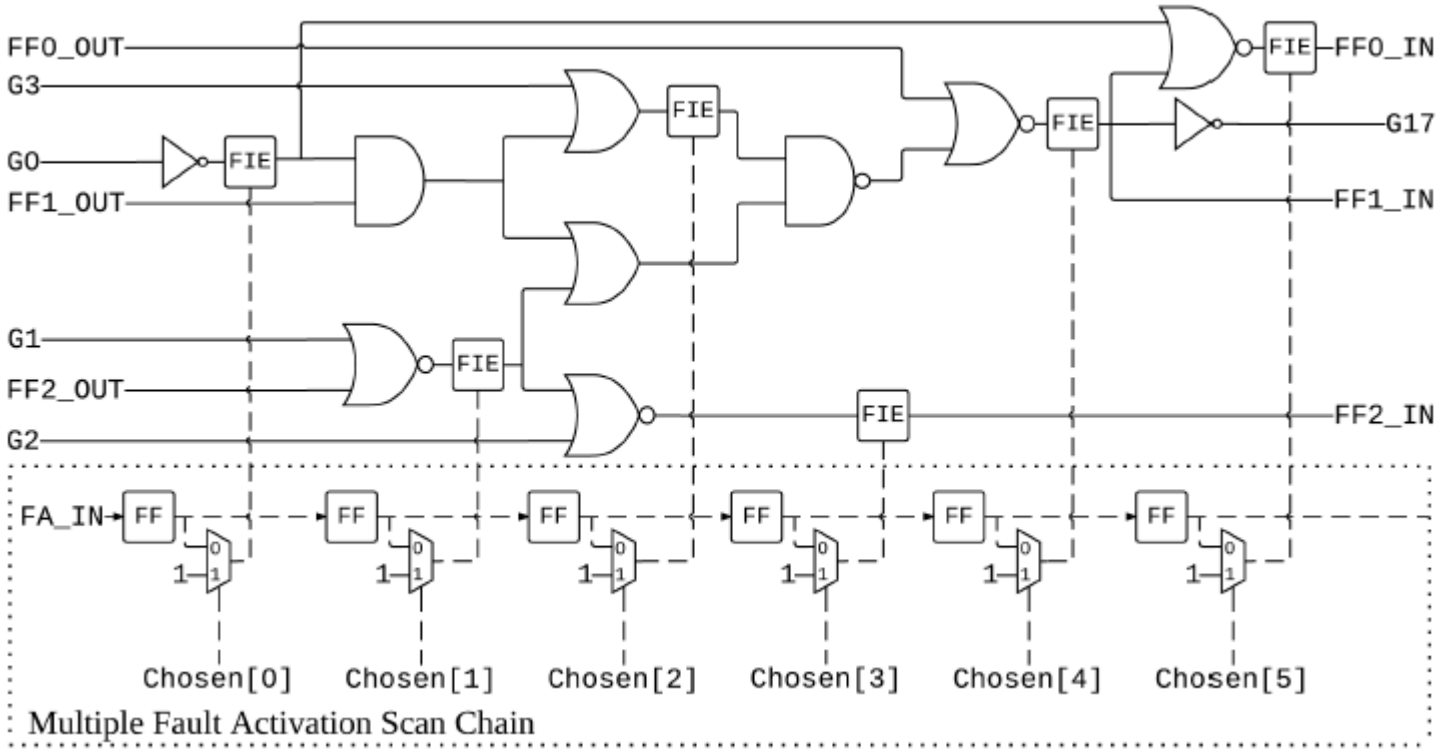


Logic Locking

- Based on fault analysis
- Renders the circuit temporarily unusable, until it is unlocked.
- Realized by inserting key-gates into the original netlist(= fault injection)



Circuit Instrumentation With Dynamic Multiple Fault Injection

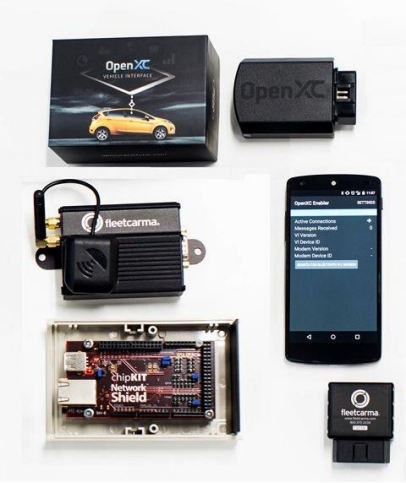


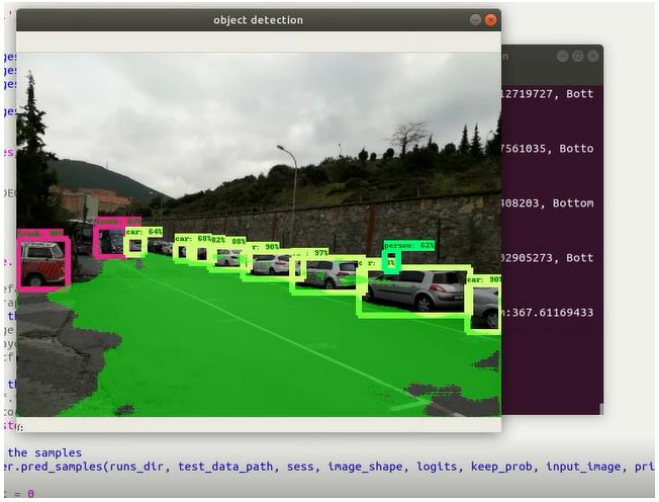
Computer Arithmetic

- Fast and Efficient Circuit Topologies for Finding the Maximum of n k-bit Numbers
- Hardware division by small integer constants
- Fast Multiplier Generator for FPGAs with LUT based Partial Product Generation and Column/Row Compression
- Lossless Look-Up Table Compression for Hardware Implementation of Transcendental Functions

Vehicular Technologies & Smart City & IoT

- Precise Vehicle Positioning for Indoor Navigation via OpenXC
- Mobile News Reader Application Compatible with In-Vehicle Infotainment
- Improving Driver Behavior Using Gamification
- Predicting Fuel Consumption via OpenXC and Machine Learning
- On-Street Parking Spot Detection for Smart Cities
- Distributed Smart Surveillance Architecture using Edge and Cloud Computing





THANK YOU